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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VU, NGOC YEN T	
ART UNIT	**PAPER NUMBER**
2612	10

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,403	TSAI, RICHARD H.	
	Examiner	Art Unit	
	Ngoc-Yen T. Vu	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 04/20/2004, have been entered and made of record. Claims 1-30 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-3, 6-8, 10-11, 13-16 and 17-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill et al. (US #6,369,853) in view of Akagawa et al. (US #5,757,008).

Regarding claim 1, Merrill '853 teaches a pixel sensor (Fig. 8), comprising an n-type photosensitive element (182) for converting an optical image to an electrical signal (col. 6 lines 28-32); a p-type source follower transistor (192) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal (col. 9 lines 20-23); a readout circuit (194) coupled to said source follower transistor (192); and a first reset circuit (184) configured to provide a reset signal at said gate of said source follower transistor (192), where said first reset

circuit includes at least one p-type transistor (col. 8 lines 46-55; col. 9 lines 13-18; col. 10 lines 1-26).

Claim 1 differs from Merrill in that the claim further requires the readout circuit comprises a p-type transistor. The limitation is well known in the art as shown in Akagawa. In the same field of endeavor, Akagawa '0088 teaches a pixel sensor (Figs. 13-15) comprising a readout circuit operating to convert optical image signals to electronic signals, wherein said readout circuit includes p-type transistors (11-14) and n-type photosensitive element (col. 21 line 65 – col. 22 line 17); and a first reset circuit (51-54) configured to reset level for a pixel output, where said first reset circuit includes at least one p-type transistor (col. 21 line 65 – col. 22 line 62). Akagawa teaches that the present invention provides an image sensor having an excellent performance with a simple circuit structure (col. 7 lines 53-56). In light of the teaching from Akagawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pixel sensor taught in Merrill by having the readout circuit comprising a p-type transistor so as to provide an image sensor having an excellent performance with a simple circuit structure.

As to claim **2**, Merrill, as modified by Akagawa, teaches that said p-type transistors are MOSFET p-type transistors (Merrill, col. 8 line 46 – col. 9 line 27) (Akagawa, col. 22 lines 1-34)

As to claim **3**, Merrill, as modified by Akagawa teaches that said n-type photosensitive element is an n-type photodiode (Merrill, col. 6 lines 28-33) (Akagawa, col. 22 lines 8-12).

As to claim **6**, Merrill, as modified by Akagawa, teaches that a p-type substrate in which said n-type photosensitive element is formed (Merrill, col. 9 lines 48+).

As to claim **7**, Merrill, as modified by Akagawa, teaches a pair of p+ type guard rings formed on said p-type substrate, each of said guard rings formed on either side of said n-type photosensitive element (Akagawa, see Figs. 7 and 9-11). Official notice is taken that it is well known in the art to connect guard rings to a ground voltage in order to reduce a leakage current from the photosensitive element.

As to claim **8**, Merrill, as modified by Akagawa, teaches an n-type well formed in said p-type substrate, said n-type well adapted for connection to a supply voltage, and operating to prevent charges from escaping the pixel sensor (Merrill, col. 7 lines 28-47, col. 8 lines 23-44).

Regarding claim **10**, Merrill '853 teaches an image sensing device (Fig. 5), comprising a p-type substrate (col. 9 lines 48+); an n-type photodiode (Fig. 8, 182) formed in said p-type substrate, where said n-type photodiode operates to convert an optical image to an electrical signal (col. 6 lines 28-32); a p-type source follower transistor (Fig. 8, 192) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal (col. 9 lines 20-23); a first reset circuit (184) configured to provide a reset signal for said electrical signal, said first reset circuit includes at least one p-type MOSFET transistor (col. 8 lines 46-55; col. 9 lines 13-18; col. 10 lines 1-26).; and a readout circuit (194) operating to buffer said electrical signal.

Claim 10 differs from Merrill in that the claim further requires the readout circuit comprises a p-type transistor. The limitation is well known in the art as shown in Akagawa. In the same field of endeavor, Akagawa '0088 teaches a pixel sensor (Figs. 13-15) comprising a readout circuit operating to convert optical image signals to electronic signals, wherein said readout circuit includes p-type transistors (11-14) and n-type photosensitive element (col. 21 line

65 – col. 22 line 17); and a first reset circuit (51-54) configured to reset level for a pixel output, where said first reset circuit includes at least one p-type transistor (col. 21 line 65 – col. 22 line 62). Akagawa teaches that the present invention provides an image sensor having an excellent performance with a simple circuit structure (col. 7 lines 53-56). In light of the teaching from Akagawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pixel sensor taught in Merrill by having the readout circuit comprising a p-type transistor so as to provide an image sensor having an excellent performance with a simple circuit structure.

As to claim **11**, the limitation in claim 11 can be found in claim 7.

As to claim **12**, Merrill, as modified by Akagawa, teaches an n-type well formed in said p-type substrate, said n-type well adapted for connection to a supply voltage, and operating to prevent charges from escaping the pixel sensor (Merrill, col. 7 lines 28-47, col. 8 lines 23-44).

Regarding claim **14**, Merrill '853 teaches a CMOS image sensor system (Figs. 5 and 8), comprising an array of active pixel sensors, each pixel sensor of said array including an n-type photosensitive element (182) operating to convert an optical image to an electrical signal (col. 6 lines 28-32); a p-type source follower transistor (192) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal (col. 9 lines 20-23); a pixel readout circuit (194) coupled to said source follower transistor (192); and a first reset circuit (184) configured to provide a reset signal at said gate of said source follower transistor (192), where said first reset circuit includes at least one p-type transistor (col. 8 lines 46-55; col. 9 lines 13-18; col. 10 lines 1-26).

a control circuit (64/74) configured to provide timing and control signals to enable readout of data stored in said array of active pixel sensors (col. 5 lines 30-56);

a column readout circuit (70) operating to receive and process said data stored in said array of active pixel sensors (col. 5 lines 30-56).

Claim 14 differs from Merrill in that the claim further requires the readout circuit comprises a p-type transistor. The limitation is well known in the art as shown in Akagawa. In the same field of endeavor, Akagawa '0088 teaches a pixel sensor (Figs. 13-15) comprising a readout circuit operating to convert optical image signals to electronic signals, wherein said readout circuit includes p-type transistors (11-14) and n-type photosensitive element (col. 21 line 65 – col. 22 line 17); and a first reset circuit (51-54) configured to reset level for a pixel output, where said first reset circuit includes at least one p-type transistor (col. 21 line 65 – col. 22 line 62). Akagawa teaches that the present invention provides an image sensor having an excellent performance with a simple circuit structure (col. 7 lines 53-56). In light of the teaching from Akagawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pixel sensor taught in Merrill by having the readout circuit comprising a p-type transistor so as to provide an image sensor having an excellent performance with a simple circuit structure.

As to claim **15**, Merrill, as modified by Akagawa, teaches that a p-type substrate in which said n-type photosensitive element is formed (Merrill, col. 9 lines 48+).

As to claim **16**, the limitation in claim 16 can be found in claim 7.

As to claim **17**, Merrill, as modified by Akagawa, teaches an n-type well formed in said p-type substrate, said n-type well adapted for connection to a supply voltage, and operating to prevent charges from escaping the pixel sensor (Merrill, col. 7 lines 28-47, col. 8 lines 23-44).

As to claims **19-20**, Merrill, as modified by Akagawa, teaches that the p-type transistor of the readout circuit comprises a row select transistor for selectively reading out said pixel output signal, and said row select transistor is coupled to receive an output of said source follower transistor (Merrill, col. 8 line 46 – col. 9 line 28) (Akagawa, col. 21 line 65 – col. 22 line 62).

As to claim **21**, Merrill, as modified by Akagawa, teaches a CMOS image sensing device and said p-type transistors provide radiation hardness without any radiation protective enclosure (Akagawa, col. 21 line 65 – col. 22 line 62).

As to claim **22**, Merrill, as modified by Akagawa, teaches that said source follower transistor (192) is a p-type MOSFET transistors (Merrill, col. 9 lines 20-23).

As to claims **23-26**, Merrill, as modified by Akagawa, teaches that the p-type transistor of the readout circuit comprises a row select transistor for selectively reading out said pixel output signal , and said row select transistor is coupled to receive an output of said source follower transistor (Merrill, col. 8 line 46 – col. 9 line 28) (Akagawa, col. 21 line 65 – col. 22 line 62).

As to claim **27**, Merrill, as modified by Akagawa, teaches a CMOS image sensing device and said p-type transistors provide radiation hardness without any radiation protective enclosure (Akagawa, col. 21 line 65 – col. 22 line 62).

5. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill ' 853 in view of Akagawa '008, and further in view of Chou (US #6,252,218).

As to claims **4-5**, the claims differ from Merrill and Akagawa in that the claims further require the photodiode is formed in a square layout design or a circular layout design. However, Chou' 218 teaches an active image sensor in which photodiodes are laid out in a geometrically-efficient patter for the purpose of increasing pixel density and pixel resolution while reducing noise and crosstalk (see Figs. 6, 7, 9 and 11; col. 4 lines 9-43). In light of the teaching from Chou, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the photodiodes as claimed in claims 4 and 5 so as to increasing pixel density and pixel resolution while reducing noise and crosstalk.

6. Claims 9, 13, 18 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill '853 in view of Akagawa '008, and further in view of Guidash (US #5,881,184).

As to claim **9**, the claim differs from Merrill and Akagawa in that the claim further requires a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allows pixel-by-pixel reset operation. However, it is well known in the art to provide a solid state image sensor with reset means which is capable of rest all pixels simultaneously as well as a pixel at a time, as taught in Guidash '184 (see Fig. 2A, col. 3 line 64 – col. 4 line 42). In light of the teaching in Guidash, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the image sensor taught in Merrill and Akagawa with a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit so as to allow all the pixels to be reset simultaneously as well as a pixel at a time.

As to claim **13**, the limitation in claim 13 can be found in claim 9.

As to claim **18**, the limitation in claim 18 can be found in claim 9.

Regarding claim **28**, Merrill '853 teaches an array of pixel sensors (Fig. 5), comprising a plurality of pixels (Fig. 8) formed in a p-type substrate (col. 9 lines 48+); at least one of said pixels comprising an n-type photodiode (Fig. 8, 182) formed in said p-type substrate and for generating an electrical signal in response to an optical image (col. 6 lines 28-32); a p-type source follower transistor (Fig. 8, 192) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal (col. 9 lines 20-23); a first reset circuit (184) coupled to said gate and responsive to a first reset signal for providing a global reset value as said pixel output signal (col. 8 lines 46-55; col. 9 lines 13-18; col. 10 lines 1-26); and a row select transistor (194) for selectively connecting the pixel to an associated column line of the array for readout of the pixel output signal (col. 8 line 46 – col. 9 line 28).

Claim 28 differs from Merrill in that the claim further requires the row select transistor comprises a p-type transistor, and a pair of p+ type guard rings formed in said p-type substrate, each of said pair of said guard rings located on either side of said n-type photodiode. The limitations are well known in the art as shown in Akagawa. In the same field of endeavor, Akagawa '0088 teaches a pixel sensor (Figs. 13-15) comprising a readout circuit operating to convert optical image signals to electronic signals, wherein said readout circuit includes p-type transistors (11-14) and n-type photosensitive element (col. 21 line 65 – col. 22 line 17); and a first reset circuit (51-54) configured to reset level for a pixel output, where said first reset circuit includes at least one p-type transistor (col. 21 line 65 – col. 22 line 62). Akagawa also teaches a pair of p+ type guard rings formed on said p-type substrate, each of said guard rings formed on either side of said n-type photodiode (Akagawa, see Figs. 7 and 9-11). Akagawa teaches that the

present invention provides an image sensor having an excellent performance with a simple circuit structure (col. 7 lines 53-56). In light of the teaching from Akagawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pixel sensor taught in Merrill by having the readout circuit comprising a p-type transistor so as to provide an image sensor having an excellent performance with a simple circuit structure.

As to claim **29**, Merrill, as modified by Akagawa, teaches an n-type well located adjacent at leas one of said pair of p+ type guard rings in said p-type substrate (Merrill, col. 7 lines 28-47, col. 8 lines 23-44) (Akagawa, see Figs. 7 and 9-11).

As to claim **30**, Merrill, as modified by Akagawa, teaches that said p-type transistors provide radiation hardness without a radiation protective enclosure (Akagawa, col. 21 line 65 – col. 22 line 62).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc-Yen T. Vu whose telephone number is 703-305-4946. The examiner can normally be reached on Mon. – Fri. from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NGOC-YEN VU
PRIMARY EXAMINER

Art Unit 2612

NYV
07/02/2004